8. The solid-state imaging device according to claim 7, wherein a third power supply wiring coupled to a drain region of the select transistor extends along the first direction.

9. The solid-state imaging device according to claim 8, wherein a signal wiring coupled to a source region of the amplification transistor extends along the first direction.

10. The solid-state imaging device according to claim 9, wherein a second connection wiring is formed in a transverse direction to connect with the select wiring.

11. The solid-state imaging device according to claim 10, wherein the second connection wiring covers an entire width of the sharing unit.

12. The solid-state imaging device according to claim 11, wherein readout wirings which are connected to readout gate electrodes are formed in the transverse direction.

13. The solid-state imaging device according to claim 12, wherein the readout wirings are formed between adjacent pixels.

14. The solid-state imaging device according to claim 2, wherein the amplification transistor has an active region comprising a source region of the amplification transistor, the drain region of the amplification transistor, and a channel region, wherein the active region extends from the source region to the drain region of the amplification transistor via the channel region, wherein the active region is formed in a cross shape, and wherein the amplification gate electrode is formed on a vertical portion of the channel region.

15. The solid-state imaging device according to claim 14, wherein a reset gate electrode of the reset transistor is formed in a transverse direction with a length of two pixel pitches.

16. The solid-state imaging device according to claim 10, wherein the first connection wiring, the second connection wiring, a select transistor power supply wiring, the select wiring, and the readout wirings are formed in a four-layer wiring structure.

17. An electronic apparatus comprising:

a solid-state imaging device comprising:

a first structural unit including a first transfer transistor group sharing a first floating diffusion, the first transfer transistor group including four transfer transistors arranged around the first floating diffusion; and

a second structural unit including a second transfer transistor group sharing a second floating diffusion, the second transfer transistor group including four transfer transistors arranged around the second floating diffusion;

wherein the first and second floating diffusions are coupled to each other in a first direction,

wherein the first and second transfer transistor groups share at least an amplification transistor and a reset transistor, the amplification transistor coupled to a select transistor,

wherein a select wiring coupled to a gate electrode of the select transistor extends along the first direction, and

wherein a first power supply wiring coupled to a drain region of the reset transistor extends along a second direction different from the first direction.

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